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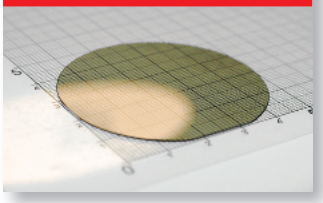
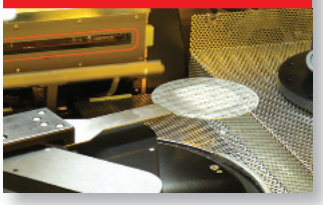
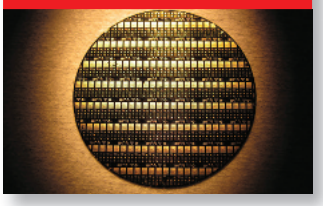
Great GaN yields better devices



Capacity hike for GaN transistors



Cooling HEMTs with diamond



Turbo-charging the VCSEL

Bigger wafers for GaN-on-silicon

Translucent

Perfecting GaN-on-silicon

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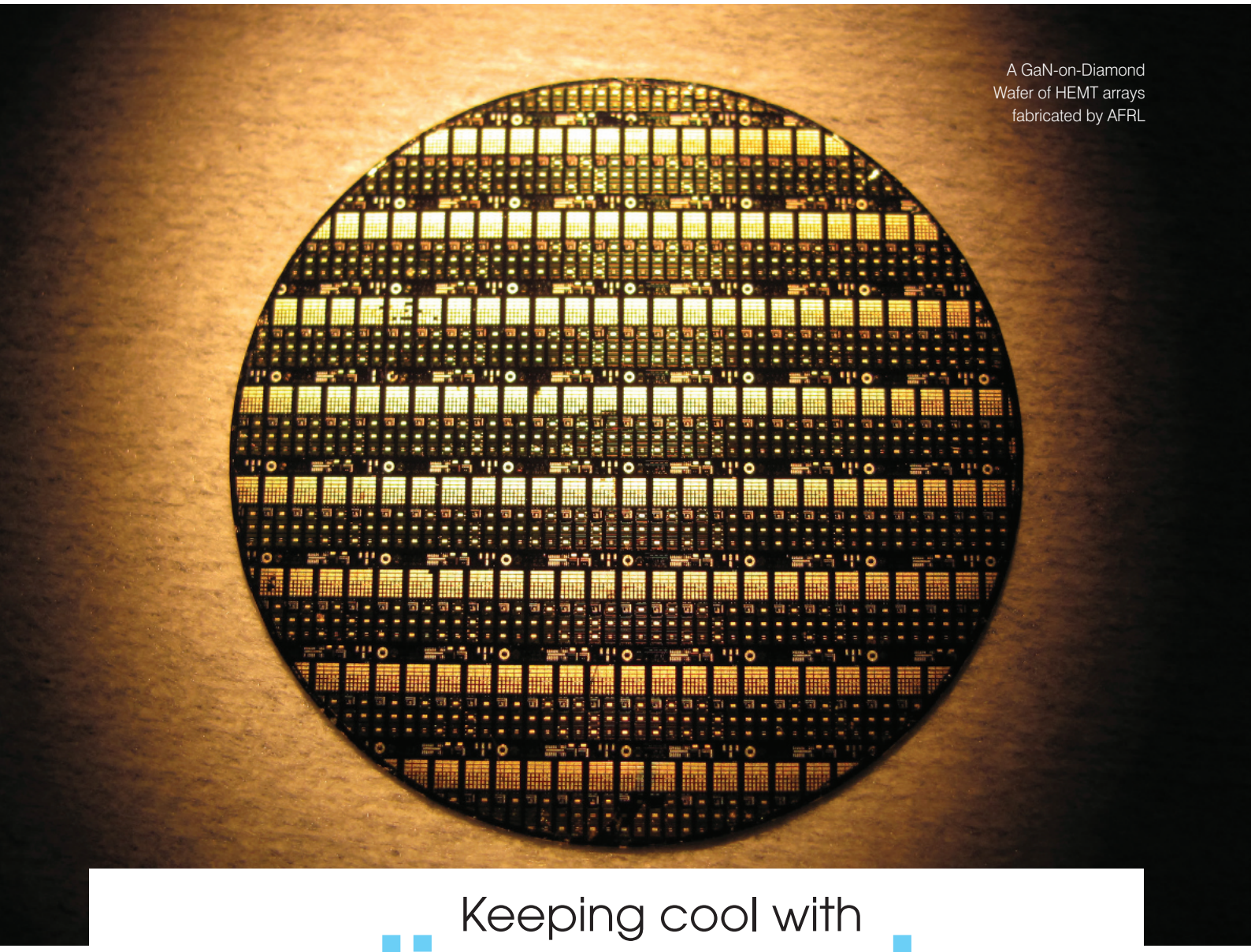

A GaN-on-Diamond Wafer of HEMT arrays fabricated by AFRL

Keeping cool with diamond

By sucking heat from GaN HEMTs better than other substrates, diamond enables transistors to operate at higher ambient temperatures and have reduced finger spacing

BY FELIX EJECKAM FROM ELEMENT SIX TECHNOLOGIES

THANKS TO A TREMENDOUS SET OF INTRINSIC CHARACTERISTICS, GaN-based RF transistors are setting a new benchmark for solid-state device performance. But that does not mean that they are fulfilling their true potential, because the heating in channel degrades device lifetime when the RF chip operates near its peak power output.

To address this weakness, our team (initially Group4 Labs, acquired by Element Six in 2013) began in 2003 to develop a higher thermal conductivity substrate that more effectively extracts heat out of a transistor based device: directly deposited CVD diamond.

This development will allow GaN-on-diamond devices to replace the more common GaN-on-SiC devices and traveling wave tubes in defence radar and electronic warfare systems. What's more, commercial systems such as cellular base stations, weather and communications satellites and power devices may be able to deliver greater energy efficiency, while being lighter and

PHYSICAL PROPERTIES OF VARIOUS BULK MATERIALS

	Si	GaAa	SiC	GaN	SAPPHIRE	CVD DIAMOND
THERMAL CONDUCTIVITY (@300K) (W/m-K)	135-150	35-50	390-450	150-250	35	1000, 1500, 2000
ELECTRICAL RESISTIVITY @ 300K (Ω-cm)	~ $2.3x10^5$	~ 10^4 - 10^8	~ 10^4-10^6	~ 10^6	~ 10^{17}	~ 10^{13}-10^{16}
YOUNG'S MODULUS (110) @ RT (GPa)	130	~ 83	~ 390-700	~ 180-200	~ 250-400	~ 1,100
DIAMETER AVAILABILITY TODAY	12"	6"	6"	1.2"	2"-4"	6"

Table 1. Electrical and thermal properties of various commercially available substrates commonly used in RF electronics or that may be used to host GaN.

smaller, due to the introduction of directly deposited diamond substrates.

One reason that the authors advocate a move to diamond is because it is the best commercial heat-spreading material in the world. It can have a room temperature thermal conductivity of more than 1500 W m^{-1} K^{-1}, and can be four-to-five times that of the next best semiconductor substrate, SiC (see table 1 for details of key physical properties of various compound semiconductors). Diamond can be deposited to within hundreds of nanometres of the GaN channel, where it can efficiently extract heat out of the transistor-based device.

Simulations, modelling, and experiments all illustrate the promise of GaN-on-diamond. Researchers from various groups, including those assembled by the Defense Advanced Research Projects Agency (DARPA), have determined that such transistor-based devices can operate at reduced channel temperatures and are capable of delivering about three times the areal power density of state-of-the-art GaN-on-SiC RF power amplifiers.

Diamond development

The first thought of turning to diamond substrates is now more than a decade old, since which there have been several key breakthroughs. They include showing that high-quality diamond substrates can be deposited on 3-inch and 4-inch GaN wafers; demonstrating that it is possible to construct RF power amplifiers incorporating our diamond technology and undertaking numerous mechanical/materials, electrical, thermal, and reliability measurements that clearly indicate the superiority of GaN-on-diamond over GaN-on-SiC in RF electronics. Unusual for a new semiconductor technology, the authors' wafer formation process has undergone very few changes during its development (see Figure 1 for a pictorial overview of the progress). However, during that time there has been an exhaustive refinement with optimization of virtually every aspect of GaN-on-diamond wafer technology. These efforts include introducing larger wafers, improving coverage yield of GaN-on-diamond, optimising the thickness of interfacial material between the GaN and diamond, reducing the wafer bow and warp and refining methods for depositing/removing protection layers on top of the GaN epitaxy.

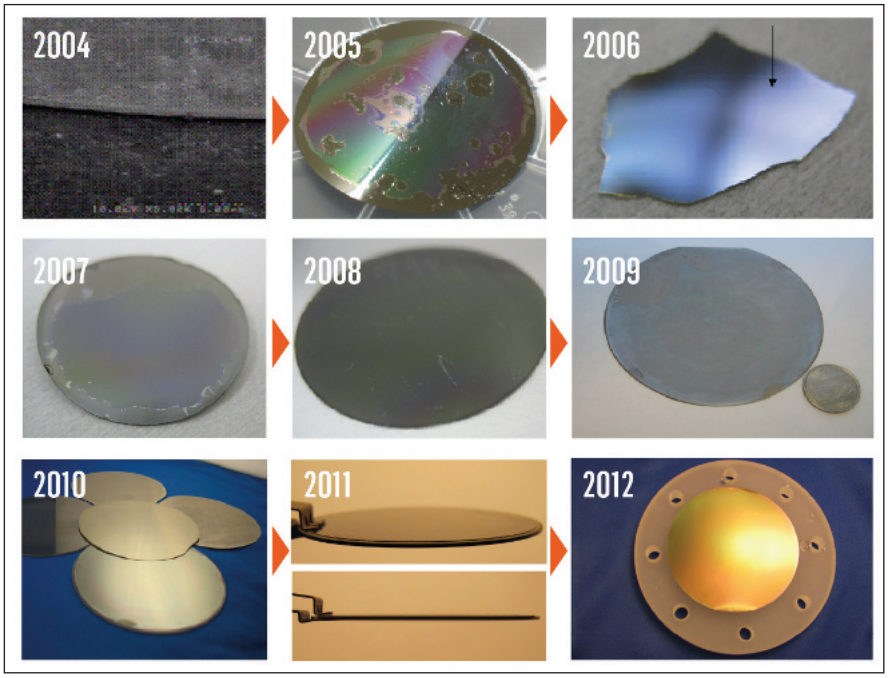

Figure 1. Development of GaN-on-diamond wafers includes the first carrier mounted 3-inch GaN-on-diamond wafer in 2011 and the first 4-inch free-standing GaN-on-diamond wafer in 2012.

GaN-on-diamond wafers (see Figure 2) are formed by first depositing the AlGaN/GaN HEMT structure by MOCVD on high resistivity silicon. The epitaxial stack includes a 1.2 μm-thick proprietary transition layer, an 800 nm-thick undoped GaN buffer layer, a 17 nm-thick $Al_{0.26}Ga_{0.74}N$ Schottky barrier and a 2 nm-thick GaN cap layer.

This epitaxial structure – GaN buffer, AlGaN barrier and GaN cap – is coated on the bottom of the GaN buffer with a dielectric and then a 100 μm-thick CVD diamond layer. This pair of additional layers is added by first removing the host silicon (111) substrate and transition layers beneath the AlGaN/GaN epitaxy, before depositing a 35 nm-thick proprietary dielectric onto the exposed AlGaN/GaN, and finally growing a 100 μm-thick CVD diamond substrate onto the dielectric adhering to the epitaxial AlGaN/GaN films.

The real test for GaN-on-diamond is whether it delivers improvement to transistor performance. This is the focus of the remainder of this article, which details two studies: The first is of a comparison of GaN-on-diamond and GaN-on-silicon HEMTs – note

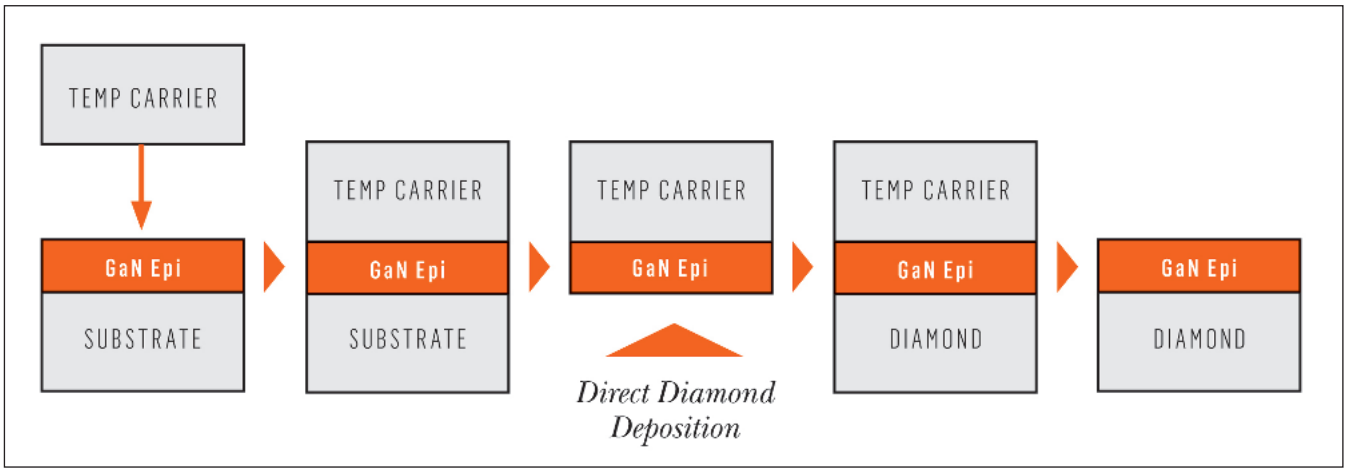

Figure 2. GaN-on-diamond structures are formed by: bonding the GaN face to a temporary carrier; etching away the substrate and transition layers; depositing a 35 nm-thick dielectric and then a diamond layer on the backside of GaN; and removing the temporary carrier.

that the GaN-on-diamond originally comes from a silicon substrate; and the second compares device performance to the GaN-on-SiC HEMT, which is the industry's prevailing GaN technology.

Recently, engineers at the US Air Force Research Laboratory (AFRL) have independently investigated whether the team's GaN epi-flip and diamond deposition process is detrimental to GaN epitaxy, and whether it can lead to any deterioration in device performance. Their examination involved the analysis of thousands of GaN-on-diamond and GaN-on-silicon HEMTs. To make the comparison as fair as possible, the GaN-on-silicon was grown at the same time as the GaN that was to be transferred to diamond. Dimensions of the HEMTs (identical on both silicon and diamond substrates) included a gate width of 300 mm (2 x 150 mm), a gate length of 0.15 mm and source-drain distance of 4.5 mm.

Epiwafers, plus devices formed from them, were scrutinised with a wide range of measurements. Entire wafers were mapped for sheet resistivity, carrier mobility, carrier density, contact resistance, sheet resistance and buffer isolation current, while measurements on passivated devices assessed values for transconductance, maximum DC drain current, saturated DC drain-source current, threshold voltage, gate leakage and knee voltage. On top of this, engineers obtained passivated RF data for the devices, including values for breakdown voltage, f_{max} (MAG), f_t, current-voltage and transfer curves. Aside from one exception – surface gate leakage – no statistically significant differences were uncovered between DC and RF measurements for GaN-on-silicon and GaN-on-diamond (see table 2 for a summary of the results).

RF performance of both types of device was then assessed with continuous-wave Maury load pull measurements at X-band (10 GHz) frequencies and various drain voltages. Select devices were matched for best power-added efficiency and biased at a quiescent drain current of 30 mA, corresponding to 100 mA/mm, in a class AB configuration. Measurements on wafers held at 25 °C on a vacuum chuck using drain voltages between 15 V and 25 V revealed that switching the foundation from silicon to diamond boosted output power by typically 1-1.5dBm and increased power-added efficiency by 7 percentage points (see Figure 3).

Engineers at AFRL also compared the current droop in both types of HEMTs. This study revealed that GaN-on-silicon HEMTs are more sensitive to pulse lengths than GaN-on-diamond HEMTs (see Figure 4), due to increased self-heating.

A combination of infrared thermography and micro-Raman techniques unveiled the thermal performance of the GaN-on-diamond and GaN-on-silicon HEMTs. Due to a 'spot-size' larger than that of the entire transistor, infrared measurements were only qualitative. These measurements made on-wafer, un-attached to a stage, involved devices operating at a drain-voltage of 25 V and drain current of 130 mA. Values for thermal resistance – the difference between the observed region's hottest temperature and that at the base of the substrate, divided by the product of the drain voltage and current – were just 7.44 K W^{-1} mm^{-1} for GaN-on-diamond HEMTs, compared with 16.6 K W^{-1} mm^{-1} and 11.5 K W^{-1} mm^{-1} for those with silicon

	GaN-ON-DIAMOND	GaN-ON-SILICON
Rc (Ω-mm)	0.36 (0.11)	0.49 (0.09)
Rsh (Ω/sq)	441 (39.4)	429 (17.8)
IISO@50V (uA)	89 (103)	226 (186)
GmPeak (mS/mm)	238 (18.6)	214 (5.3)
Vth (V)	-3.58 (0.04)	-3.81 (0.05)
Imax (mA/mm)	813 (56.3)	697 (39.6)
Idss (mA/mm)	707 (58.6)	617 (57.3)
Igl (uA/mm)	-5.66 (5.49)	-0.56 (0.84)
Vbk (V)	25.75 (10.64)	27.94 (5.02)
GLag@5V (%)	7.9 (NA)	7.1 (NA)
Dlag@5V (%)	10.0 (NA)	10.6 (NA)

Table 2. A summary of average (and standard deviation) DC and RF measurements made by AFRL on identically designed GaN-on-diamond and GaN-on-silicon HEMTs.

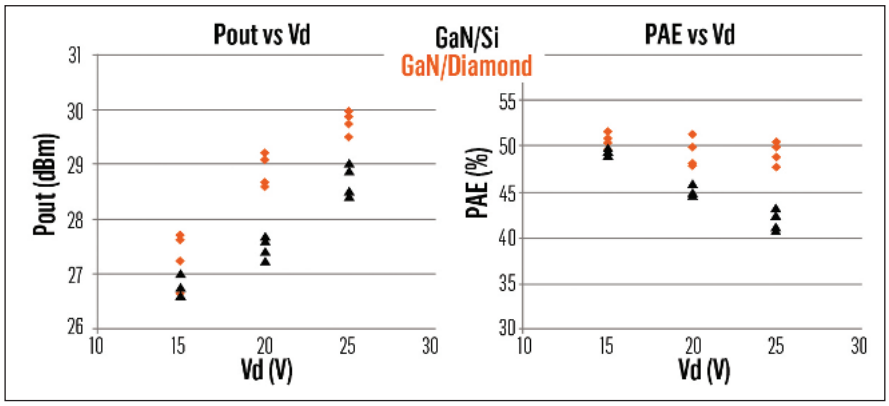

Figure 3. X-band load-pull measurements taken from GaN-on-diamond and GaN-on-silicon HEMTs across multiple levels of power dissipation.

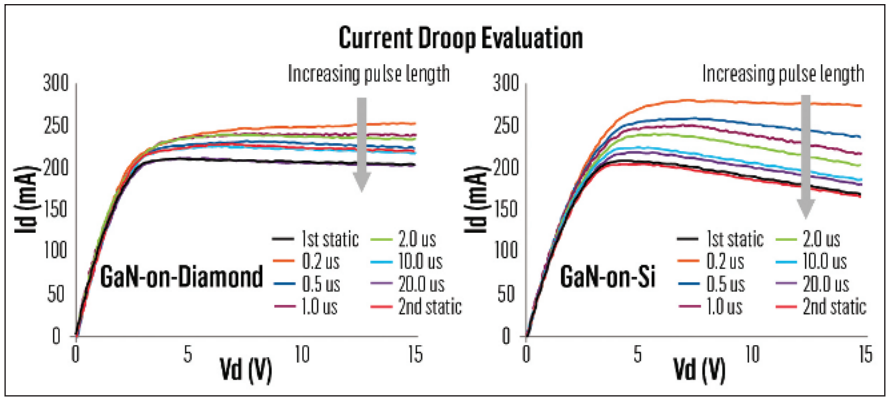

Figure 4. Current droop measured from GaN-on-diamond (left chart) and GaN-on-silicon HEMTs (right chart) across various duty-cycles.

devices, with a gate-to-gate spacing of 10 mm and 40 mm for GaN-on-diamond and 30 mm and 40 mm for GaN-on-SiC (see Figure 7). Gate temperatures were measured in all these devices, which had a common packaging configuration and operated at multiple power dissipation levels.

Simulations suggest that for a similar peak channel temperature, GaN-on-diamond HEMTs can employ one-third of the gate-to-gate spacing of GaN-on-SiC equivalents, thanks to a 40 percent reduction in channel-to-substrate thermal resistance.

To verify this, engineers probed thermal characteristics with micro-Raman thermography and gate thermometry (see Figure 8). Both of these techniques are not capable of measuring the true peak temperature that occurs in the HEMT, so peak temperatures are simulated – these represent the hottest nodal temperature in the HEMT finite element model. Confidence in the peak-temperature calculations derives from a good agreement between the model, the gate thermometry and the micro-Raman measurements. HEMT temperatures determined via measurement of gate forward bias voltage, which is calibrated

and SiC foundations, respectively. Quantitative measurements of thermal resistance are possible with micro-Raman thermal analysis, which has a spot volume of about 1 mm^3 from the GaN surface into the buffer.

Temperatures measured between the gate and drain (nearer the former) as well as near the edge of the diamond substrate, led to values for thermal resistance of about 8.0 K W^{-1} mm^{-1} for the GaN-on-diamond HEMT (see Figure 6). In comparison, GaN-on-silicon equivalents exhibited thermal resistance of about 21 K W^{-1} mm^{-1}.

Comparisons with SiC

For high-power GaN RF applications, the industry's leading substrate is SiC. So, it is the performance of HEMTs built on this platform that set the benchmark against which GaN-on diamond devices should be judged. Engineers at Raytheon have compared these two classes of device, using 10 x 125 mm HEMTs formed with the company's microwave GaN process. This study involved forming a portfolio of

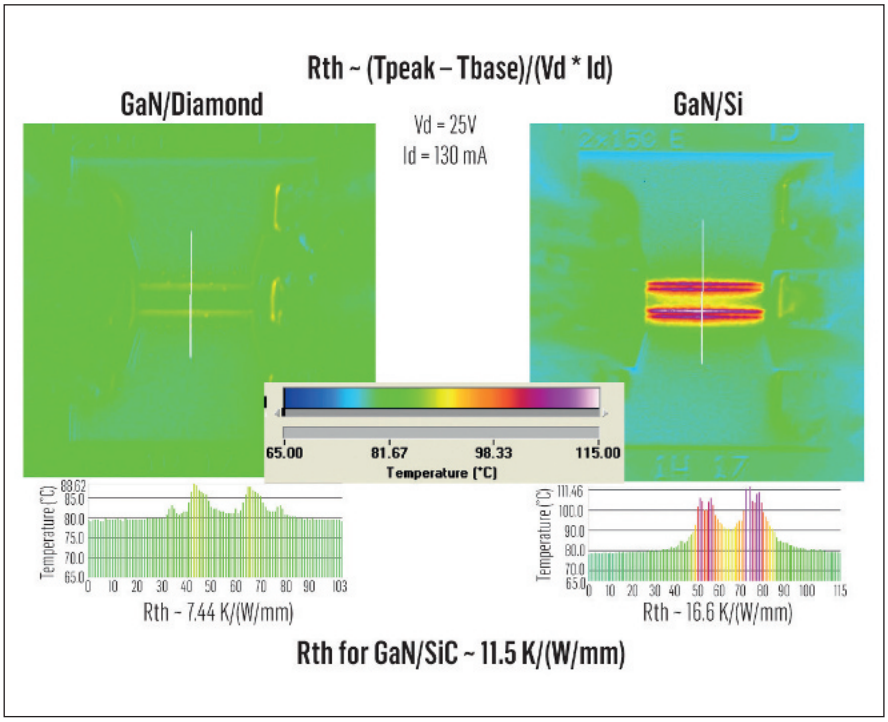

Figure 5. An infrared image of GaN-on-diamond and GaN-on-silicon HEMTs under bias. The temperature difference between the device's gate and the base of the substrate was used in the calculations.

to temperature, are in good agreement with simulations. They show that at a dissipated power of 4.2 W/mm, the peak junction temperature of the 10 mm gate-to-gate GaN-on-diamond HEMT is just 6.3 °C (6 percent) higher than the 30 mm gate-to-gate GaN-on-SiC device. And for 40 mm gate-to-gate spacings at 4.2 W/mm dissipated power, the GaN-on-diamond device has a junction temperature 8.5°C lower than the GaN-on-SiC equivalent. These efforts also reveal that switching from SiC to diamond delivers a spike in areal dissipation density from 140 W/mm^2 to 420 W/mm^2.

These results are for an early generation of GaN-on-diamond structures. Measurements on more recent material show that thermal performance has improved, which should result in even more impressive devices.

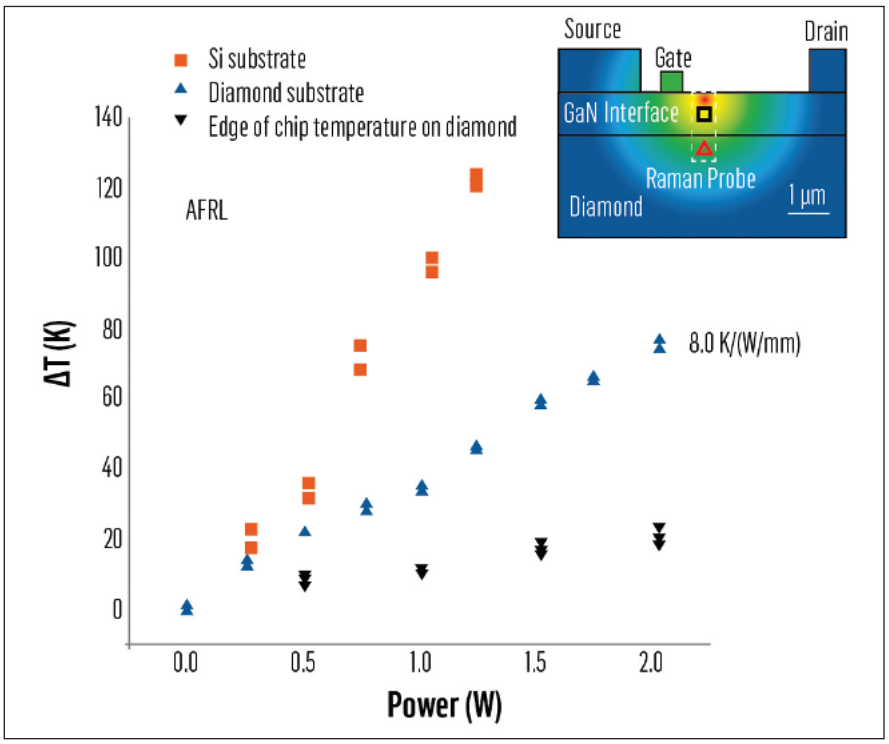

Figure 6. Temperature change measured for GaN-on-diamond and GaN-on-silicon HEMTs using a micro-Raman technique.

Is GaN-on-diamond reliable?

The introduction of any new substrate will always bring concerns over reliability. With diamond, scepticism can stem from its significant differences, compared to GaN, in its thermal expansion coefficient, crystal structure, surface properties and internal stress. To put these concerns to bed, the authors have subjected GaN-on-diamond HEMTs to channel temperatures of up to 350°C using a constant source-drain voltage of 24 V.

A series of endurance tests involved monitoring the source-drain currents and gate leakage currents of batches of devices operated for thousands of hours at elevated channel temperatures. Currents for the GaN-on-diamond HEMTs deviated by less than 25 percent of their starting values after: 4,000 hours at 350°C, 9,000 hours at 290°C and 17,000 hours at 210°C. In contrast, all the control GaN-on-silicon devices, which share the same GaN epitaxy and device structure as their GaN-on-diamond cousins, catastrophically failed within a few hundred hours of the start of the tests.

Apparently, removal of the highly defective transition layers between GaN and silicon, prior to diamond deposition, contributed to the improvements resulting from the introduction of GaN-on-diamond. However, to confirm that this is the case, more research is warranted to better understand these results. Trimming the thermal resistance by 40 percent by switching from GaN-on-SiC to GaN-on-diamond should have two major benefits on the design of radar, electronic warfare, defence radio, communications and weather satellites, cellular base stations, and naval avionics systems: it should cut cooling complexity and cost, and it should deliver a three-fold increase in the areal power density of the GaN transistor.

Reductions in cooling complexity and cost are possible when thermal resistance falls, because less stringent demands are placed on the coolant temperature. This can open the door to simpler, cheaper thermal management

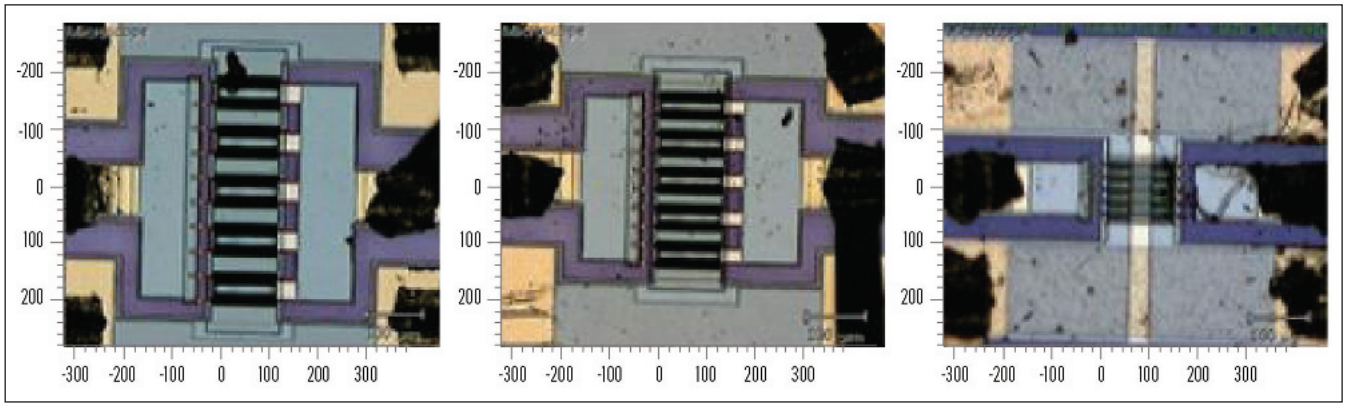

Figure 7. GaN HEMTs characterized by micro-Raman and gate thermometry techniques. From left: GaN-on-SiC 40 micron gate-to-gate spacing, GaN-on-SiC 30 micron gate-to-gate spacing, and GaN-on-diamond 10 micron gate-to-gate spacing.

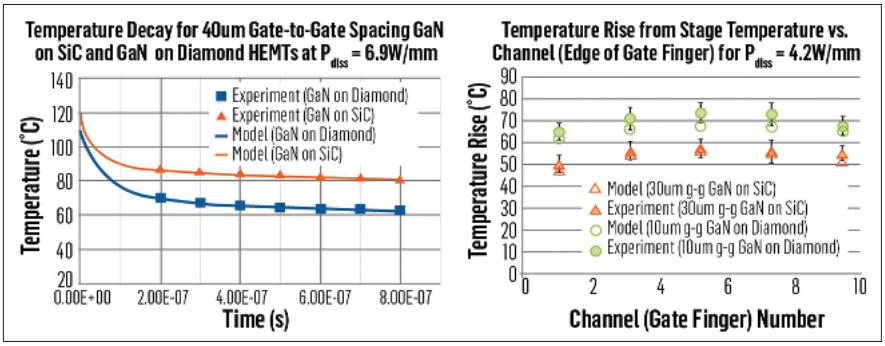

Figure 8. A comparison of simulations and experimental values for the temperatures for GaN-on-SiC and GaN-on-diamond HEMTs. Experiments involved gate thermometry (left) and micro-Raman (right) techniques. On the left, GaN-on-diamond and GaN-on-SiC HEMTs are compared with equivalent gate-to-gate spacing and dissipation (6.9 W/mm). On the right, the GaN-on-diamond HEMT has a threefold reduction in gate-to-gate spacing relative to the GaN-on-SiC HEMT.

systems; and it can also enable higher coolant (or device operating) temperatures, because the temperature rise from the coolant to the gate is lower. The higher areal power densities that are possible with the reduced thermal resistance of GaN-on-diamond derive from a shrinking of gate finger separation by a factor of three, leading to smaller, cheaper GaN-on-diamond devices.

For the manufacturers of power amplifier chips, processing three times fewer GaN-on-diamond wafers than GaN-on-SiC variants, while maintaining the same total RF output power, leads to significant reductions in fab costs – assuming that commercial GaN-on-diamond wafers are competitively priced to GaN-on-SiC wafers. And if the GaN-on-diamond wafer price is low enough, then vendors' power amplifier savings can be passed on to the system maker, reducing the power amplifier price per watt.

This is an attractive scenario, showcasing the opportunity for GaN-on-diamond technology to deliver revolutionary advantages for system performance and cost, which can make it the ideal choice for next-generation HEMTs.

Many people have contributed to the work described in this article: Daniel Francis, Firooz Faili, Frank Lowe, Tim Mollart, Joe Dodson, Daniel Twitchen and Bruce Bolliger from Element Six Technologies; Dubravko Babic from the University of Zagreb; Quentin Diduck from Avogy; Chandra Khandavalli from iMata Technologies; Matthew Tyhach, David Altman and Steve Bernstein from Raytheon Company and Samuel Graham from Georgia Institute of Technology.

The views expressed are those of the author and do not reflect the official policy or position of the Department of Defense or the US Government.

Contributions to GaN-on-diamond development

Key milestones in GaN-on-dimaond development:

- In 2005, DARPA's award to Group4 Labs, Inc. of the first seed contract to demonstrate a 10 mm x 10 mm piece of GaN-on-diamond wafer. DARPA would provide instrumental funding later on – via the Near Junction Thermal Transport effort under DARPA's Thermal Management programme to characterize the thermal benefits of the new technology. P1 Diamond and Crystallume Corporation grew the first wafers for the team in 2004 and 2005, respectively.
- In 2006, the first-ever operational transistor on a GaN-on-diamond wafer. The transistors were made by Wright Patterson Air Force Research Labs.
- The US Missile Defense Agency awarding the first of many SBIR programs. TriQuint Semiconductor and Raytheon Company were the first commercial entities to demonstrate operational GaN-on-diamond transistors. The US Navy SBIR program was the first to fund a reliability-related programme with the team in 2009.
- In 2009, Element Six SA – the largest synthetic diamond maker in the world – becoming an instrumental backer of GaN-on-diamond. Element Six subsequently enabled scale-up of the technology after acquiring Group4 Labs in 2013.

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