GaN-on-Diamond HEMT Technology with T_{AVG} = 176 °C at $P_{DC,max}$ = 56 W/mm Measured by Transient Thermoreflectance Imaging

Marko J. Tadjer, *Senior Member, IEEE,* Travis J. Anderson, *Senior Member, IEEE,* Mario G. Ancona, Peter E. Raad, *Senior Member, IEEE,* Pavel Komarov, Tingyu Bai, James C. Gallagher, Andrew D. Koehler, *Member, IEEE,* Mark S. Goorsky, Daniel A. Francis, Karl D. Hobart, *Senior Member, IEEE,* and Fritz J. Kub, *Life Fellow, IEEE*

***Abstract*—Record DC power has been demonstrated in AlGaN/GaN high electron mobility transistors fabricated using a substrate replacement process in which a thick diamond substrate is grown by chemical vapor deposition following removal of the original Si substrate. Crucial to the process is a ~30 nm thick SiN interlayer that has been optimized for thermal resistance. The reductions obtained in self-heating have been quantified by transient thermoreflectance imaging and interpreted using 3D numerical simulation. With a DC power dissipation level of 56 W/mm, the measured average and maximum temperatures in the gate-drain access region were 176 °C, and 205 °C, respectively.**

***Index Terms*— GaN, diamond, thermoreflectance, thermal management, transmission electron microscopy**

I. Introduction

GaN-based high electron mobility transistors (HEMTs) have been of critical importance for commercial and military applications which require the high frequency and high power density enabled by the wide bandgap and high critical field of gallium nitride. However, the long-term reliability of GaN at high power has continued to face unique challenges originating from the simultaneous high electric field and high temperature within the channel of a GaN HEMT [1, 2]. It was envisioned early on that the thermal limitations of GaN rf devices could be addressed by utilizing CVD diamond with its high thermal conductivity to provide an efficient heat extraction path between the III-nitride heterostructure and the heat sink [3-6]. And indeed early GaN-on-Diamond technology, realized by wafer bonding with a thin bonding layer, was able to outperform GaN-on-SiC [7]. While direct bonding of GaN and diamond has continued to improve, GaN-on-diamond technology has focused on removal of the Si substrate and the AlGaN nucleation layers, followed by thick CVD diamond overgrowth [8, 9]. This approach, despite leading to excellent reports of full-wafer GaN-on-Diamond HEMTs, has also faced multiple compatibility challenges which so far have prevented the commercialization of a GaN-on-diamond technology [10, 11]. In this work, we demonstrate significant improvements in thermal performance of GaN-on-diamond HEMTs resulting from a high quality interface between these two materials.

Manuscript received March 2, 2019.

M.J. Tadjer, T.J. Anderson, M.G. Ancona, J.C. Gallagher, A.D. Koehler, K.D. Hobart, and F.J. Kub are with the U.S. Naval Research Laboratory, Washington DC, 20375, USA (marko.tadjer@nrl.navy.mil).

P.E. Raad is with the Southern Methodist University, Dallas TX, and TMX Scientific, Richardson TX. P. Komarov is with TMX Scientific, Richardson, TX. T. Bai and M.S. Goorsky are with the University of California, Los Angeles, CA. D.A. Francis is with Akash Systems, Inc., San Francisco, CA.

II. Experimental

The diamond substrate replacement process began by attaching an inverted GaN-on-Si wafer to a temporary carrier, removing the Si, and then etching the N-polar III-nitride nucleation layers until an approximately 700 nm thick GaN buffer was obtained. After depositing a thin (~30 nm) SiN barrier layer, thick polycrystalline CVD diamond was seeded and grown by Element Six Technologies (E6) using a proprietary process [11-13]. The final step was detaching the carrier leaving the GaN-on-Diamond wafer.

The HEMT devices had 20nm of $Al_{0.2}Ga_{0.8}N$ and were fabricated simultaneously on wafers both before and after substrate replacement as follows: Cl-ICP mesa etch, Ti/Al/Ni/Au Ohmic contacts, rapid-thermal anneal (850°C, 30s, N_2), Ni/Au Schottky gates, Ti/Au overlay pads, 100 nm thick mixed-frequency PECVD SiN passivation optimized for low current collapse [14]. Using this approach, two GaN-on-Diamond samples were identified from an early and a more mature version of the process (GaNDi-1 and GaNDi-2, respectively) and an electrothermal comparison was carried out using the reference samples, GaNSi-1 and GaNSi-2.

The HEMTs were characterized electrically and with steady state and transient thermoreflectance imaging (TRI) performed on a TMX Scientific T°Imager® system with a 100X near-UV objective at 365 nm illumination wavelength, and calibrated by a 330-450 nm scan that confirmed the optimal response from each sample. Temperature change was derived from the reflectivity change ($\Delta T = (\Delta R/R)/C_{TR}$), where C_{TR} is the temperature-dependent pixel-by-pixel calibrated coefficient of thermoreflectance [15, 16]. Broadband dark acquisition under relatively low drain bias showed that the electroluminescence (EL) signal had a negligible intensity of less than 0.1% of the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2019.2909289, IEEE Electron Device Letters

Table I. Summary of relevant electrothermal characteristics for samples GaNSi-1, GaNSi-2, GaNDi-1 and GaNDi-2.

Sample	R_{SH} (Ω/□)	μ_{HALL} (cm^2 / V-s)	N_{SH} ($x10^{12}$ cm^{-2})	$I_{D,MAX}$, V_{GS}=1V (A/mm)	V_{TH} (V)	$I_{D,OFF}$ -10V_{DS} (mA)	$I_{G,REV}$ -10V_{DS} (mA)	G_M (mS / mm)	R_{ON} (Ω-mm)	R_{TH} (°C-mm /W)	τ (ns)
GaNSi-1	678	1520	6.06	0.15	-1.4	<0.01	<0.01	77.2	10.21	12.9	1120
GaNSi-2	526	1443	8.22	0.46	-3.0	0.19	-0.28	82.6	9.01	4.5	960
GaNDi-1	625	1588	6.29	0.45	-3.4	36.7	-0.058	52	9.56	3.91	150
GaNDi-2	484	1367	9.44	0.48	-2.9	1.49	-2.7	75.7	9.12	2.95	161

thermoreflectance signal value. Accuracy in ΔT was 1°C for more than 95% of the data acquired and analyzed in image post-processing. Transient TRI used a square V_{GS} pulse (-2.2 V≤V_{GS}≤0 V) and a DC V_{DS} bias.

III. Results and Discussion

Table I summarizes the electrothermal characteristics of the samples in this experiment. Room temperature Hall measurements and DC I-V characteristics indicated that the substrate-side process did not significantly influence the mobility and sheet carrier density, and thus the on-resistance of the HEMTs. Additionally, only minimal effects on threshold voltage and transconductance were observed [17].

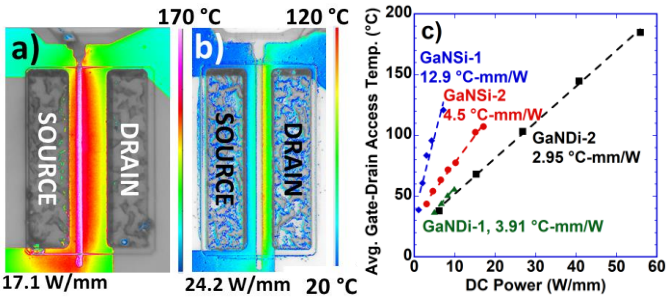

Fig. 1. Steady-state thermoreflectance maps of AlGaN/GaN HEMTs before and after backside diamond deposition process measured at 365nm illumination as a function of DC output power. a) Sample GaNSi-2. b) Sample GaNDi-2. c) Average temperature in the gate-drain access region as a function of DC power (I_{DS}xV_{DS}) for the AlGaN/GaN HEMTs in Table I.

A comparison of steady-state thermal performance was carried out as a function of DC power (I_{DS}×V_{DS}). TRI maps for GaNSi-2 and GaNDi-2 are presented in Fig. 1a-b for comparable DC power density values. The temperature profile above 15W/mm of sample GaNSi-2 extended throughout the 20µm long access region, indicating that the temperature in the metal contacts can increase beyond 150°C, leading to reliability concerns in the absence of a thermal substrate. By contrast, no significant increase in temperature was measured on GaNDi-2 near the contacts for power densities as high as 24.2W/mm (Fig. 1b). Above this power level, gate leakage current added a significant parasitic component to the total drain current (10-15%, depending on the device) but even in its presence the average temperature in the access region did not exceed 176°C (Fig. 1c), while T_{MAX} was measured to be 205±3.8°C in the hot spot near the drain edge of the gate.

The thermal profile of each sample as a function of DC power density is shown in Fig. 1c. The corresponding thermal resistance per unit width (henceforth referred to simply as the thermal resistance) was calculated from the slope of each curve. A low thermal resistance value of 2.95°C-mm/W was calculated for sample GaNDi-2. By comparison, sample GaNDi-1 exhibited a thermal resistance of 3.91°C-mm/W due to defects at the interface with the diamond substrate, as discussed below.

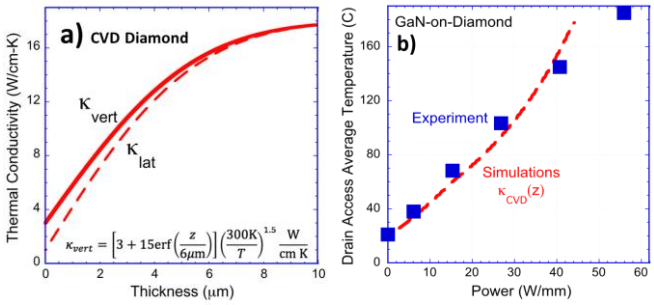

Fig. 2. a) Thickness (z) dependent lateral and vertical thermal conductivity for nanocrystalline diamond (NCD) developed using references samples of NCD on Si. b) Experimental and simulated average steady-state temperature as a function of DC power for sample GaNDi-2.

The steady-state thermal resistance of sample GaNDi-2 was verified by 2D electrothermal simulation performed using Comsol®[18], where model details have been described elsewhere [19]. The thermal conductivity of the diamond substrate was assumed to be thickness-dependent and anisotropic as shown in Fig. 2a [20-24]. Using the thermal boundary resistance (TBR) at the GaN/diamond interface as a fitting parameter (20m^2 K/GW), reasonable agreement between experiment and simulation can be obtained in steady state as seen in Fig. 2b. The upward slope of the simulated curve is due to the increase in κ_{CVD} with temperature. Above 40 W/mm, uncertainty in the temperature dependence of κ_{CVD}, TBR, and C_{TR} in the samples compared to those used by Comsol® and TImager®, as well as the onset of gate leakage current in the on state, will affect agreement between measured and simulated temperatures in high-power GaN-on-diamond HEMTs.

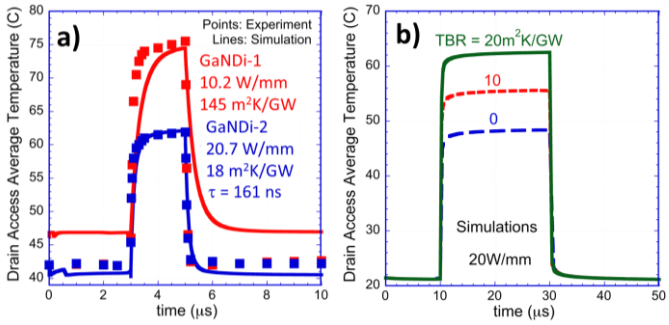

Fig. 3. a) Measured and simulated transient temperature profiles comparing sample GaNDi-1 at 10.2 W/mm and GaNDi-2 at 20.7 W/mm using only the GaN/diamond TBR as a fitting parameter. b) Simulated effect of thermal boundary resistance (TBR) reduction on the transient thermal behavior of AlGaN-GaN HEMT on diamond at 20 W/mm output power.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2019.2909289, IEEE Electron Device Letters

The transient thermoreflectance technique also enabled the measurement of temperature fields in the time domain. A square pulse (10μs period, 50% duty cycle) applied to the gates of GaNDi-1 and GaNDi-2 HEMTs with identical geometry resulted in significantly lower T_{AVE} in sample GaNDi-2 (Fig. 3a), even at twice the power level. Similar values for the thermal decay time constant were measured for both GaN-on-diamond samples with exponential decay fitting (Table I). Good agreement with transient thermal simulation for GaNDi-2 at 20 W/mm was obtained using essentially the same TBR value (18 m^2K/GW) as in Fig. 2b. Fitting the data for sample GaNDi-1 required a TBR of 145 m^2K/GW, suggesting that interface defects dominated the cooling rate in that device. Further improvement in transient thermal performance will be achieved as the GaN/diamond interface and the thermal conductivity of CVD diamond near the interface improve (Fig. 3b) [25, 26].

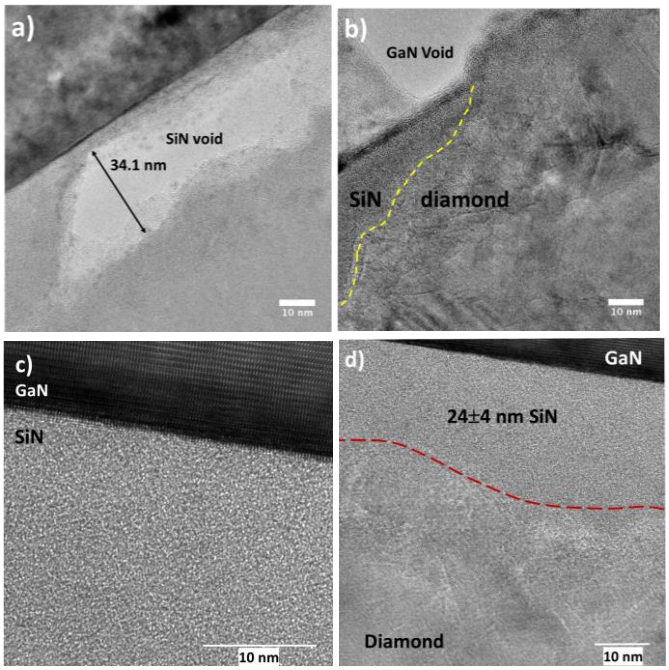

Fig. 4. High resolution TEM micrographs of the GaN/SiN/diamond interface of a) sample GaNDi-1 showing a void in the SiN, b) sample GaNDi-1 showing a void in the N-polar side of the GaN caused by H-plasma etching during diamond CVD, c) sharp, void-free interface between amorphous SiN and crystalline GaN for sample GaNDi-2, and d) SiN/polycrystalline diamond substrate interface for sample GaNDi-2 (delineated by the dashed red line).

High-resolution TEM imaging of the interfaces was performed on the two generations of GaN-on-diamond devices to help understand the measured differences in thermal performance. For the earlier generation sample (GaNDi-1), nm-sized voids in both the SiN barrier (Fig. 4a) and the GaN near the interface (Fig. 4b) were observed in addition to a rough interface where the SiN barrier layer that was completely consumed in some places. By contrast, the more recent generation sample (GaNDi-2) exhibited a significantly improved quality of the interface (Fig. 4c) where an amorphous 24±4 nm thick SiN film preserved the N-polar GaN side from being etched by the H plasma, achieving a sharp GaN-diamond interface and lower thermal resistance.

This result highlights the importance of preserving the barrier dielectric at the GaN/diamond interface. In Ref. 26, Middleton et al. reported thermal boundary resistance values using Element Six GaN-on-diamond HEMTs with a 700 nm and a 350 nm thick GaN buffer and interface dielectric thickness of 36 and 17 nm, respectively, resulting in thermal resistances of 4.2 and 2.61 K-mm/W for those samples. While the R_{TH}=3.91 °C-mm/W measured on sample GaNDi-1 compared very well to the 4.2 K-mm/K value in Ref. 26, we show that an R_{TH} < 3 K-mm/K could be obtained by using a thinner SiN layer and keeping the GaN buffer relatively thick, potentially improving frequency performance in rf GaN-on-diamond HEMTs. Thermal simulation without the SiN barrier reduced R_{TH} by an additional 48%, confirming our hypothesis that optimizing diamond growth on N-polar GaN will drive future performance improvements for this technology.

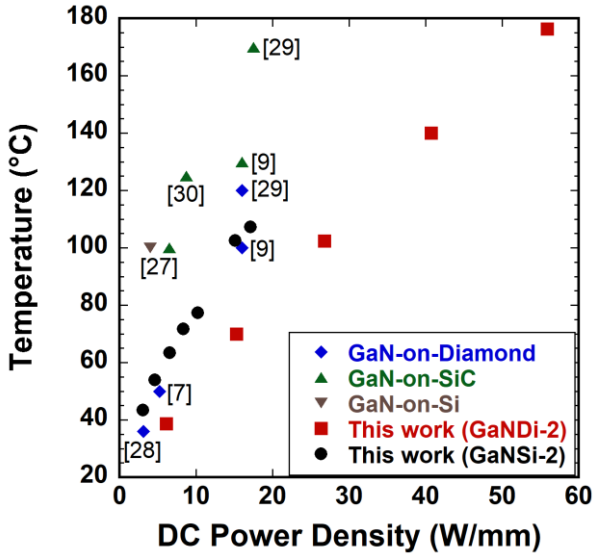

Fig. 5. Thermal performance of GaN HEMTs before (●) and after (■) diamond substrate in this work, benchmarked against earlier generations of GaN-on-Si (▼), GaN-on-SiC (▲), and GaN-on-diamond (♦) [27-30].

IV. Summary and Conclusions

This study provides the first direct comparison of GaN HEMTs before and after diamond substrate integration. High DC output power, combined with low measured channel temperature demonstrate the potential of GaN-on-Diamond technology for very high power (>50W/mm) GaN technology. Figure 5 shows samples GaNSi-2 and GaNDi-2 benchmarked against earlier GaN HEMT thermal management reports [7, 9, 27-31]. Despite the high leakage current in our devices, which still limits their breakdown voltage, we demonstrate that from a thermal standpoint the CVD diamond substrate can absorb the heat generated in the HEMT channel as long as a low-TBR thermal path is provided by the fabrication process. Thus, a high-quality diamond growth process on N-polar GaN is most critical for optimizing this interface and maximizing GaN-on-Diamond technology performance.

Acknowledgment

The authors are sincerely grateful to Element Six for providing GaN-on-Diamond HEMT samples, and the NRL Nanoscience Institute staff for cleanroom support. Research at NRL was supported by the Office of Naval Research.

REFERENCES

[1] J.D. Albrecht, P.P. Ruden, S.C. Binari, M.G. Ancona, "AlGaN/GaN heterostructure field-effect transistor model including thermal effects," IEEE Electr. Dev. Lett., vol. 47, pp. 2031, 2000.

[2] D.J. Meyer, T.I. Feygelson, T.J. Anderson, J.A. Roussos, M.J. Tadjer, B.P. Downey, D.S. Katzer, B.B. Pate, M.G. Ancona, A.D. Koehler, K.D. Hobart, C.R. Eddy, Jr., "Large-Signal RF Performance of Nanocrystalline Diamond Coated AlGaN/GaN High Electron Mobility Transistors," IEEE Electr. Dev. Lett., vol. 35, pp. 1013-1015, 2014.

[3] M. Seelmann-Eggebert, P. Meisen, F. Schaudel, P. Koidl, A. Vescan, H. Leier, "Heat-spreading diamond films for GaN-based high-power transistor devices," Diamond Relat. Mater., 10, 744, 2001.

[4] F. Ejeckam, D. Francis, F. Faili, D. Twitchen, B. Bolliger, D. Babic, J. Felbinger, "GaN-on-Diamond: A Brief History," Proc. Lester Eastman Conf. on High Perf. Dev., 2014. DOI: 10.1109/LEC.2014. 6951556, and references therein.

[5] K.D. Chabak, J.K. Gillespie, V. Miller, A. Crespo, J. Roussos, M. Trejo, D.E. Walker, G.D. Via, G.H. Jessen, J. Wasserbauer, F. Faili, D.I. Babic, D. Francis, F. Ejeckam, "Full-Wafer Characterization of AlGaN/GaN HEMTs on Free-Standing CVD Diamond Substrates," IEEE Electr. Dev. Lett., vol. 31, no. 2, pp. 99, 2010.

[6] M.J. Tadjer, T.J. Anderson, K.D. Hobart, T.I. Feygelson, J.D. Caldwell, C.R. Eddy, Jr., F.J. Kub, J.E. Butler, B.B. Pate, J. Melngailis, "Reduced Self-Heating in AlGaN/GaN HEMTs Using Nanocrystalline Diamond Heat-Spreading Films," IEEE Electr. Dev. Lett., vol. 33, no. 1, pp. 23, 2012.

[7] J. Felbinger, M.V.S. Chandra, Y. Sun, L.F. Eastman, J. Wasserbauer, F. Faili, D. Babic, D. Francis, F. Ejeckam, "Comparison of GaN HEMTs on Diamond and SiC Substrates," IEEE Electr. Dev. Lett., vol. 28, no. 11, pp. 948, 2007.

[8] F. Mu, R. He, T. Suga, "Room temperature GaN-diamond bonding for high-power GaN-on-diamond devices," Scripta Materialia, vol. 150, pp. 148-151, 2018.

[9] J.W. Pomeroy, M. Bernardoni, D.C. Dumka, D.M. Fanning, M. Kuball, "Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping," Appl. Phys. Lett 104, 083513 (2014)

[10] D. Liu, D. Francis, F. Faili, C. Middleton, J. Anaya, J.W. Pomeroy, D.J. Twitchen, M. Kuball, "Impact of diamond seeding on the microstructural properties and thermal stability of GaN-on-diamond wafers for high-power electronic devices," Scripta Materialia 128, 57 (2017)

[11] [Online]. Available: https://akashsystems.com/technology/

[12] D.C. Dumka, T.M. Chou, F. Faili, D. Francis, F. Ejeckam, "AlGaN/GaN HEMTs on diamond substrate with over 7 W/mm output power density at 10 GHz," Electr. Lett. vol. 49, no. 20, pp. 1298-1299, 2013.

[13] H. Sun, R.B. Simon, J.W. Pomeroy, D. Francis, F. Faili, D.J. Twitchen, M. Kuball, "Reducing GaN-on-diamond interfacial thermal resistance for high power transistor applications," Appl. Phys. Lett., vol. 106, pp. 111906, 2015.

[14] M.J. Tadjer, T.J. Anderson, A.D. Koehler, C.R. Eddy, Jr., D.I. Shahin, K.D. Hobart, F.J. Kub, "A Tri-Layer PECVD SiN Passivation Process for Improved AlGaN/GaN HEMT Performance," ECS Jour. Solid State Sci Technol. 6, P58-P61, 2017.

[15] M. G. Burzo, P. L. Komarov, P. E. Raad, "Non-Contact Transient Temperature Mapping of Active Electronic Devices Using the Thermoreflectance Method," *IEEE Trans. Components and Packaging Tech.*, vol. 28, pp. 637-643, 2005

[16] P.E. Raad, P.L. Komarov, M.G. Burzo, "Thermal characterization of embedded electronic features by an integrated system of CCD thermography and self-adaptive numerical modeling," Microelectr. J., vol. 39, pp. 1008-1015, 2008.

[17] M.J. Tadjer, T.J. Anderson, J.C. Gallagher, P.E. Raad, P. Komarov, A.D. Koehler, K.D. Hobart, F.J. Kub, "Thermal Performance Improvement of GaN-on-Diamond High Electron Mobility Transistors," Dev. Res. Conf. Proc., 2018. DOI: 10.1109/DRC.2018.8442138.

[18] [Online]. Available: http://www.comsol.com

[19] M.G. Ancona, S.C. Binari, D.J. Meyer, "Fully coupled thermoelectro-mechanical analysis of GaN high electron mobility transistor degradation," J. Appl. Phys. 111, 074504 (2012).

[20] R.B. Simon, J. Anaya, F. Faili, R. Balmer, G.T. Williams, D.J. Twitchen, M. Kuball, "Effect of grain size of polycrystalline diamond on its heat spreading properties," Appl. Phys. Express, vol. 9, pp. 061302, 2016.

[21] L. Yates, J. Anderson, X. Gu, C. Lee, T. Bai, M. Mecklenburg, T. Aoki, M.S. Goorsky, M. Kuball, E.L. Piner, S. Graham, "Low Thermal Boundary Resistance Interfaces for GaN-on-Diamond Devices," ACS Appl. Mater. Interfaces, vol. 10, pp. 24302, 2018.

[22] J. Philip, P. Hess, T. Feygelson, J.E. Butler, S. Chattopadhyay, K.H. Chen, L.C. Chen, "Elastic, mechanical, and thermal properties of nanocrystalline diamond films," J. Appl. Phys. 93, 2164 (2003).

[23] J. Anaya, S. Rossi, M. Alomari, E. Kohn, L. Tóth, B. Pécz, K.D. Hobart, T.J. Anderson, T.I. Feygelson, B.B. Pate, M. Kuball, "Control of the in-plane thermal conductivity of ultra-thin nanocrystalline diamond films through the grain and grain boundary properties," Acta Materialia 103, 141-152 (2016).

[24] J.E. Graebner, S. Jin, G.W. Kammlott, B. Bacon, L. Seibles, W. Banholzer, "Anisotropic thermal conductivity in chemical vapor deposition diamond," J. Appl. Phys. 71, 5353 (1992).

[25] A. Sood, R. Cheaito, T. Bai, H. Kwon, Y. Wang, C. Li, L. Yates, T. Bougher, S. Graham, M. Asheghi, M. Goorsky, K.E. Goodson, "Direct Visualization of Thermal Conductivity Suppression Due to Enhanced Phonon Scattering Near Individual Grain Boundaries," Nano Lett., vol. 18, no. 6, pp. 3466, 2018.

[26] C. Middleton, H. Chandrasekar, M. Singh, J.W. Pomeroy, M.J. Uren, D. Francis, M. Kuball, "Impact of thinning the GaN buffer and interface layer on thermal and electrical performance in GaN-on-diamond electronic devices," Appl. Phys. Expr. 12, 024003 (2019).

[27] S. Martin-Horcajo, A. Wang, M.-F. Romero, M.J. Tadjer, F. Calle, "Simple and Accurate Method to Estimate Channel Temperature and Thermal Resistance in AlGaN/GaN HEMTs," IEEE Trans. Electr. Dev., vol. 60, no. 12, pp. 4105, 2013

[28] K. Hirama, Y. Taniyasu, M. Kasu, "AlGaN/GaN high-electron mobility transistors with low thermal resistance grown on single-crystal diamond (111) substrates by metalorganic vapor-phase epitaxy," Appl. Phys. Lett., vol. 98, pp. 162112, 2011.

[29] D.C. Dumka, T.M. Chou, J.L. Jimenez, D.M. Fanning, D. Francis, F. Faili, F. Ejeckam, M. Bernardoni, J.W. Pomeroy, M. Kuball, "Electrical and Thermal Performance of AlGaN/GaN HEMTs on Diamond Substrate for RF Applications," IEEE Comp. Semicond. Intergrated Circuit Symp. (CSICS), 2013. DOI: 10.1109/CSICS.2013.6659225.

[30] M. Kuball, J.M. Hayes, M.J. Uren, T. Martin, J.C.H. Birbeck, R.S. Balmer, B.T. Hughes, "Measurement of Temperature in Active High-Power AlGaN/GaN HFETs Using Raman Spectropscopy," IEEE Electr. Dev. Lett., vol. 23, no. 1, pp. 7, 2002.