Electrical and Thermal Performance of AlGaN/GaN HEMTs on Diamond Substrate for RF Applications

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***Abstract* — Thermal conductivity of the substrate affects the performance of high power RF devices. It is a dominant limiting factor in current state-of-the-art GaN HEMTs on SiC substrate. Due to high thermal conductivity, diamond substrate is an attractive alternative for GaN HEMTs. We have developed device quality GaN-on-diamond wafers using CVD diamond and fabricated 0.25 µm gate length HEMTs. We present detailed electrical and thermal results of the fabricated devices, which show RF power comparable to standard GaN-on-SiC HEMTs. We demonstrate over 25 % lower channel temperature for these devices compared to GaN-on-SiC devices. Electrical results using DC and RF tests and thermal results using IR thermography and micro-Raman spectroscopy are included.**

***Index Terms* — AlGaN/GaN, GaN-on-diamond, CVD Diamond, HEMT, 10 GHz, RF Power, Electrical, Thermal**

I. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) on SiC substrates have been reported with extremely high RF power densities reaching 40 W/mm [1]. Such capabilities of AlGaN/GaN heterostructure, however, cannot be exploited for real applications without developing aggressive and novel thermal management techniques to control the channel temperatures so that the devices can operate reliably. Although the SiC substrate with its good thermal conductivity (350-400 W/m-K) is an attractive choice for high power GaN HEMTs, it is not good enough to take the full advantage of GaN [2]. Further, the epitaxial growth defects at the interface of GaN and SiC make it worse for thermal performance [3]. Consequently, today's discrete HEMTs in production are typically limited to the power densities of around 5-7 W/mm, while same devices are further restricted below 5 W/mm when used in high power MMIC amplifiers [4].

To address the above problem and make use of untapped RF power of GaN, we have been investigating AlGaN/GaN HEMTs on high thermal conductivity polycrystalline diamond substrates. Using this approach, we have recently reported a record of over 7 W/mm RF power for GaN-on-diamond HEMTs at 10 GHz [5]. In this paper, we present detailed electrical and thermal performance evaluation of GaN-on-diamond HEMTs. We demonstrate that compared to SiC, diamond substrate for GaN HEMTs allows over 25% reduction in channel temperature at the same power dissipation level.

II. MATERIAL AND DEVICE FABRICATION

To prepare the GaN-on-diamond device wafers (Fig. 1), the AlGaN/GaN HEMT layer structure was first grown by metal-organic chemical vapor deposition (MOCVD) on a high resistivity Si (111) substrate. Device wafers were then prepared by first removing the host Si (111) and transition layers beneath the AlGaN/GaN epitaxy, depositing a 50 nm thick proprietary dielectric onto the exposed AlGaN/GaN, and finally growing 100 µm-thick polycrystalline diamond using a chemical vapor deposition (CVD) process onto the dielectric adhered to the epitaxial AlGaN/GaN films. GaN-on-diamond wafers were temporarily mounted on the carrier wafers for device processing. Using the contactless Lehighton measurement, an average sheet resistance of 440 Ω/ϒ was measured on the wafers. HEMTs were fabricated using a dielectrically defined 0.25 µm gate-length process. HEMT fabrication steps included mesa isolation, Ohmic contacts, gate process, dielectric passivation and overlay metallization.

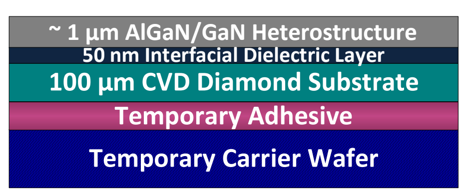

Fig. 1. Schematic cross-section of GaN-on-diamond device wafer mounted on a temporary carrier for processing.

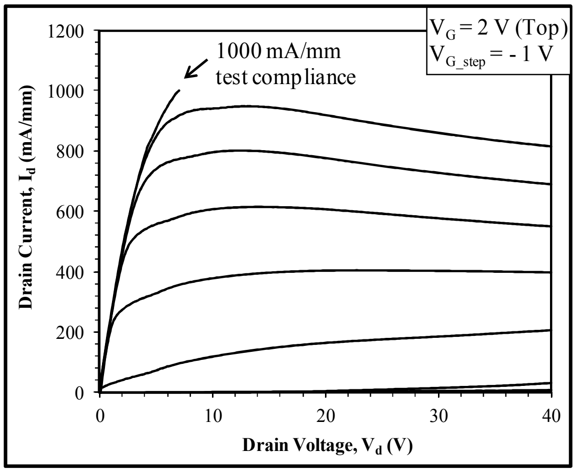

Fig. 2. Drain current characteristics of a 50 µm gate-width GaN HEMT on diamond.

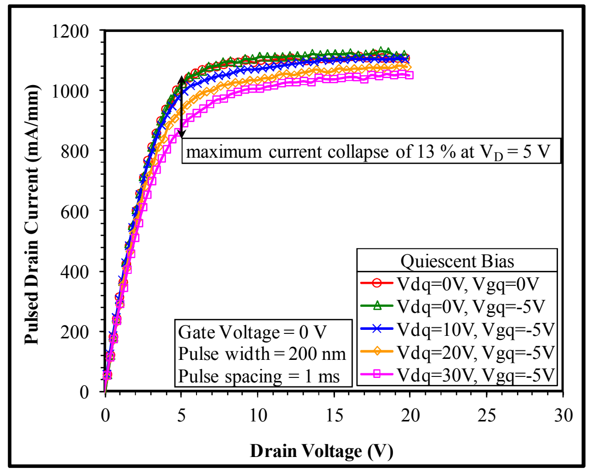

Fig. 3. Pulsed I-V characteristics of a 2x100 µm gate-width GaN HEMT on diamond at various quiescent conditions.

Source-drain spacing of 4 µm was used. Test HEMTs with gate peripheries from 50 µm to 200 µm and Transfer Length Measurement (TLM) test structures were fabricated for electrical and thermal characterization.

III. MEASUREMENTS AND RESULTS

Electrical and thermal measurements of various test structures were performed on-wafer.

A. Electrical Measurements and Results

DC characteristics of the test HEMTs were measured using an Agilent Semiconductor Parameter Analyzer. Current-voltage (I-V) curves of a 50 µm gate width HEMT up to a high drain voltage of 40 V, plotted in Fig. 2, show promising and robust drain current characteristics along with a maximum current density of 1 A/mm. Threshold voltage of -3.4 V and peak DC transconductance in excess of 280 mS/mm were measured for these devices at 10 V of drain voltage. Gate-drain breakdown voltage was between 25 V and 50 V at 1 mA/mm of gate-drain current. It was low as gate leakage current was high possibly due to the processes that GaN surface was exposed to during the wafer preparation.

Pulsed I-V tests were performed using DIVA test set up to evaluate current collapse (CC) in the fabricated devices. Fig. 3 shows the measured pulsed I-V of a 2x100 µm HEMT. A pulse width of 200 ns and pulse spacing of 1 ms are used. Testing is performed at several quiescent bias conditions. Device is pulsed to a fixed gate voltage of 0 V while drain voltage is varied from 0 to 20 V, and the corresponding drain current is recorded. Curve for quiescent bias V_{dq} = V_{gq}= 0 V is used as a reference to determine the CC at 5 V drain voltage. It can be seen that the device did not show any CC when pulsed from a pinched-off state of V_{gq} = -5 V while V_{dq} = 0 V. CC increases with V_{dq}. However, even at a maximum V_{dq} of 30 V, CC is only 13 % which is comparable to that of standard GaN-on-SiC devices. These results are promising for good RF performance of these devices.

Small signal s-parameters of 2x100 µm HEMTs were measured using Agilent 8510C network analyzer. Cut-off frequency (f_t) of 30 GHz was determined at a drain voltage of 30 V and drain current density of 150 mA/mm.

Using Focus load-pull set up, measured RF power performance of 2x100 µm HEMTs at 10 GHz is shown in Fig. 4. Devices were biased at different drain voltages of

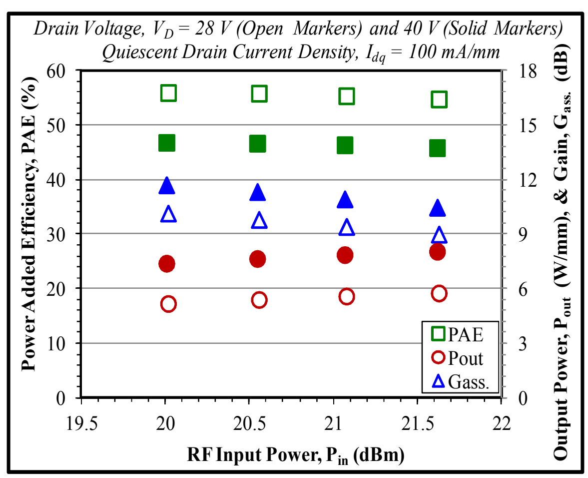

Fig. 4. 10 GHz load pull results of a 2x100 µm GaN HEMT on diamond at different bias conditions.

28 V and 40 V while keeping a fixed quiescent drain current density of 100 mA/mm. Input-output power response was recorded for each test condition. It can be seen that devices reach over 7 W/mm output power at 40 V bias, which is a record performance for GaN-on-diamond HEMTs at 10 GHz. This is achieved with over 46 % power-added efficiency (PAE). At 28 V, an output power of over 5 W/mm along with the PAE of about 55 % is achieved. The output power achieved in these devices is comparable to that of standard GaN-on-SiC HEMT. PAE of these GaN-on-diamond HEMTs is affected by high gate leakage current, and significant improvement in PAE is expected by leakage reduction.

B. Thermal Measurements and Results

Thermal performance evaluation of GaN-on-diamond devices was done using micro-Raman spectroscopy and IR thermography techniques. Test HEMTs with gate width of 2x100 µm and TLM structures with 100 µm width and 20 µm spacing were used to measure the channel temperature rise at different DC power dissipation conditions. For comparison, TriQuint's standard 100 µm-thick 2x100 µm GaN-on-SiC HEMT was also tested using micro-Raman technique. Details of micro-Raman technique are presented by Pameroy et. al [6]. IR measurements were done using QFI-IR Infrascope II with a spatial resolution of 5 µm. Baseplate temperature in IR tests was fixed at 70 °C.

For GaN-on-diamond HEMTs, an average temperature rise of 23 K/W was measured using IR thermography as shown in Fig. 5. On the other hand, an average temperature rise of 34 K/W using micro-Raman spectroscopy was recorded as shown in Fig. 6. For the same size GaN-on-SiC reference HEMT, micro-Raman measurements showed an average temperature rise of 41 K/W as illustrated in Fig. 7. The difference between IR and micro-Raman technique is possibly due to partial transparency of the diamond substrate. We are continuing efforts to better understand the reason of this difference. To be on the conservative side, we are using the micro-Raman data for channel temperature assessment. Using the micro-Raman data, the peak channel temperatures were simulated. It is determined by micro-Raman analysis that for the same power dissipation the GaN-on-diamond HEMT shows over 25% lower temperature rise than that of GaN-on-SiC. This is a significant improvement, which is attributed to the thermal resistance reduction of GaN-

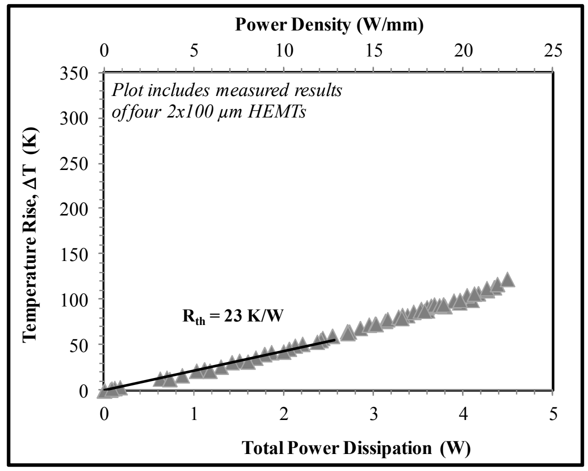

Fig. 5. Temperature rise of 2x100µm GaN HEMTs on diamond with DC power dissipation measured using an IR camera.

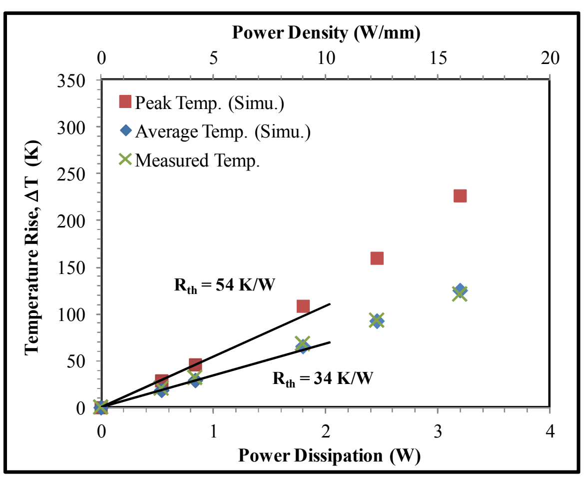

Fig. 6. Temperature rise of a 2x100µm GaN HEMT on diamond with DC power dissipation as measured by micro-Raman and as simulated by fitting the measured data.

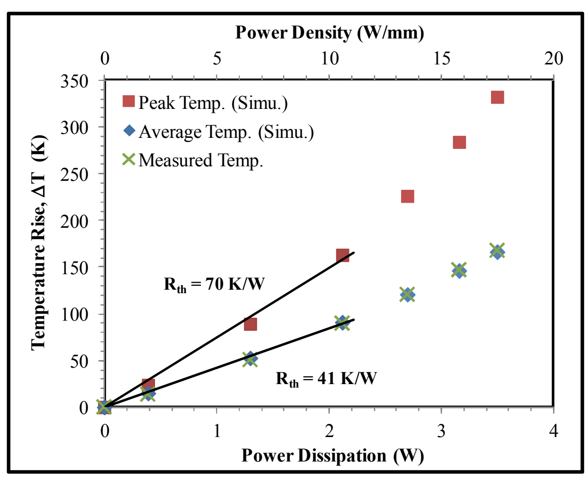

Fig. 7. Temperature rise of a standard 2x100µm GaN HEMT on SiC with DC power dissipation as measured by micro-Raman and as simulated by fitting the measured data.

on-diamond by means of high thermal conductivity of diamond in the close vicinity (~1 μm) of the hot GaN HEMT junction and removal of defective transition layer of GaN-on-Si beneath the AlGaN/GaN films.

Further, the GaN and diamond interface is considered crucial for the reduction of thermal resistance. In order to determine the thermal boundary resistance (TBR) at GaN and diamond interface, micro-Raman tests of the TLM patterns (20 μm spacing and 100 μm width) were performed. Temperature was measured at the GaN and diamond layers near the interface and depth profile of the temperature across the interface was simulated and fitted to the measured data as shown in Fig. 8. The thermal boundary resistance (TBR) of GaN-on-diamond was determined to be $1.8\text{x}10^{-8}$ m^2K/W. This yielded a thermal conductivity of 2.8 W/m-K for the GaN and diamond interface including the dielectric layer.

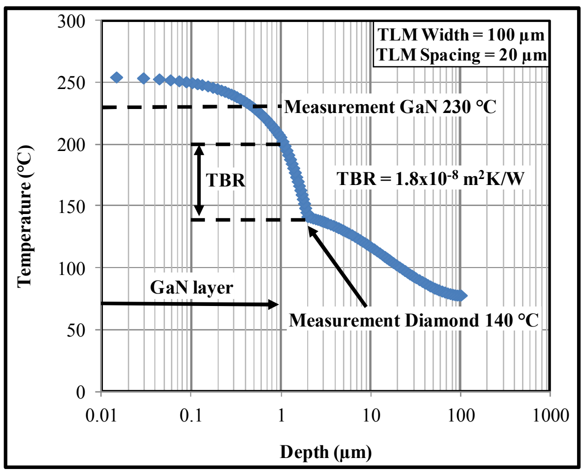

Fig. 8. Depth profile of temperature of a GaN-on-diamond TLM structure using micro-Raman measurements and simulation.

VII. Conclusion

We have presented a detailed electrical and thermal performance evaluation of GaN-on-diamond HEMTs. Device wafers have been developed by removing the host Si (111) substrate and transitions layers of GaN-on-Si wafer and subsequently depositing 50 nm dielectric and 100 μm thick CVD diamond layer. Very promising DC characteristics are achieved for HEMTs with maximum current densities in excess of 1 A/mm and operation up to 40 V. Further development is needed to improve the gate leakage current. These devices achieve a record RF power for GaN-on-diamond HEMTs at 10 GHz. Significant improvement of PAE is expected with reduction of leakage current. Further, thermal measurements confirmed over 25 % lower channel temperature rise for GaN-on-diamond HEMTs compared to a standard GaN-on-SiC HEMTs at a fixed power dissipation condition. This significant improvement shows the promise that GaN-on-diamond approach holds for advancing the GaN technology to significantly higher power levels.

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