175,000 Device-Hours Operation of AlGaN/GaN HEMTs on Diamond at 200°C Channel Temperature

Dubravko I. Babić, *Senior Member*, Quentin Diduck, *Member*, Chandra S. Khandavalli, Daniel Francis, Firooz N. Faili, *Member*, and Felix Ejeckam

***Abstract*—Hundred and seventy-five thousand device-hours of operating life at channel temperatures above 200°C is demonstrated on AlGaN/GaN HEMTs fabricated using GaN-on-diamond technology for the first time. No catastrophic failures and no drain-current drift larger than 10% from turning the devices on were recorded throughout this two-year DC test**.

***Index Terms*—diamond, gallium nitride, semiconductor device reliability, transistors**

I. Introduction

THE introduction of new semiconductor-device technologies carries a burden of proof that not only their performance and price can offer advantages over exiting technologies, but that the devices exhibit reliability sufficient for commercial deployment. The interest in AlGaN/GaN high-electron mobility transistors (HEMT) as potential work-horse of high-power RF and power-management applications has spurred great interest in their reliability [1], [2], [3]. AlGaN/GaN HEMTs are traditionally fabricated on sapphire, silicon carbide, or silicon. Growing GaN on these heterogeneous substrates necessitates the incorporation of nucleation layers between the substrate and the high-quality GaN epilayers. This approach carries multiple disadvantages from thermal management point of view: some substrates have poor thermal conductivity, while the nucleation layers exhibit significant thermal boundary resistance in addition to their low bulk thermal conductivity (< 25 W/mK) resulting from the high dislocation density and use of AlGaN ternary alloys. The recent attempts to minimize or alleviate some of these problems comprise attempts to integrate GaN with diamond [4], [5], [6], [7], [8], [9]. The approach of Group4 Labs, in which GaN epilayers are atomically attached to chemical-vapor deposited (CVD) diamond wafers has up to now exhibited great progress by demonstrating 100-mm GaN-on-diamond wafers [10], devices with f_T ~ 85 GHz [11], and X-band amplifiers [12]. GaN-on-diamond technology not only replaces the original, growth substrate with diamond but it also allows the removal of the poorly thermally conductive nucleation layers prior to attaching the epilayers to diamond.

The reliability of devices built by processes in which epilayers are transferred from the growth substrate to another substrate, such as, epitaxial liftoff, wafer bonding, and atomic attachment, understandingly undergo special scrutiny of the components community because mechanical handling of thin epilayers is more likely to introduce damage and stresses to the semiconductor epilayers and/or the device than traditional semiconductor fabrication in which the epilayers stay attached to the as-grown substrate. In addition, atomic attachment relies on several high-temperature process steps. Therefore, the central question posed by many interested users of this technology is whether GaN-on-diamond devices will last. This paper contains the first report of high-temperature operating life (HTOL) experiments on GaN-on-diamond high-electron mobility transistors.

The primary objective of this experiment was to check whether these devices would "last through the weekend". The result was surprising, as up to date over 175,000 device-hours have been collected on devices that operate with channel temperatures above 200°C, I_{DS} ~ 60 mA/mm, and V_{DS} up to 48 V. We describe the device design, the experimental setup, and the results of the first two-year operating life test on GaN-on-diamond HEMTs.

II. Device Structures and Life-Test Details

AlGaN/GaN high-electron mobility transistors (HEMT) were fabricated on GaN-on-diamond wafers with layer structure shown in Figure 1. Gallium-nitride on silicon wafers were purchased with standard epilayer design from Nitronex, Inc. and the GaN epilayers were transferred onto diamond using Group4 Labs' atomic attachment process [10]. The wafers used in this work were of the first generation of GaN-on-diamond devices in which the nucleation layers (shown in Figure 1**)** are still present. The wafers were processed at MicroGaN in Ulm, Germany. Free-standing GaN-on-diamond wafer diameter was 24 mm and the wafers were attached to 100-mm silicon wafers for processing.

The layout contained a variety of two gate HEMTs with no air-bridges. The gate metallization was Ni/Au, while silicon nitride was used for passivation. Device physical dimensions

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Dubravko I. Babić, Quentin Diduck, Chandra S. Khandavalli, Daniel Francis, Firooz Faili, Felix Ejeckam are with Group4 Labs, Inc., Fremont, California, CA 94539. (e-mail: dubravko.babic@group4labs.com).

were $W = 2 \times 400$ µm, $L_G = 1.2$ and 2 µm, $L_{GD} = 3$, 4, and 5 µm. We could not resolve the effect of these dimensional variations on the performance nor the reliability, hence, in the test we treated the devices as being identical. The wafers were diced using Q-switched Nd:YAG laser [13]. The final chip size was 1.5 x 1.5 mm and it contained two HEMTs per chip. The chips were packaged into Stratedge 580286 packages using silver epoxy. The reason for silver epoxy was that solder could not wet the rough diamond back-surface; the back of the diamond wafer on these experimental devices was not coated with metal. The package lid was omitted.

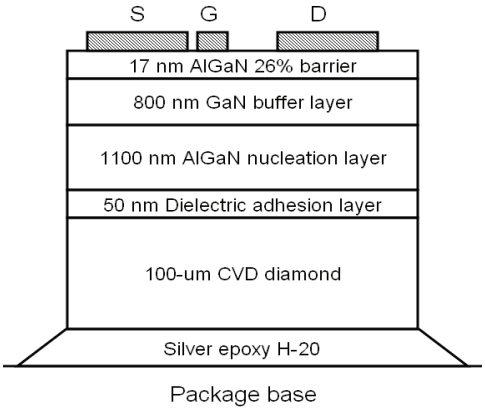

Figure 1 – GaN-on-diamond HEMT epilayer structure

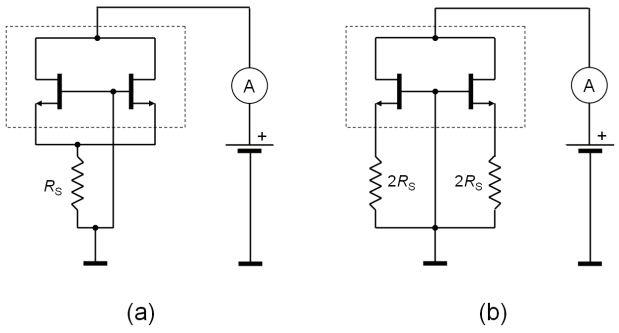

Figure 2 – Electrical wiring: (a) common source resistor, and (b) separate source resistors. The two transistors in the dashed-line box represent the two halves of a two-source HEMT on a chip.

The devices were self-biased according to the electrical scheme shown in Figure 2 which allows biasing and real time measurement of I_{DS} at constant V_{DS} with a single wire per device (also: single power supply and one meter per device). The transistor was stabilized using short bondwires and negative feedback (R_S) chip resistors inside the package. The two electrical circuit diagrams shown in Figure 2 are equivalent provided that the two sides of the two-gate transistors have identical DC characteristics. We first used diagram from Figure 2(a) with $R_S = 25$ Ω (Table 1, Groups 1-3), but subsequently realized that the circuit layout with two separate sources, common to microwave transistors, enables one to use separate source DC operating point stabilizing resistors R_S as shown in Figure 2(b) and photo in Figure 3. Using separate source resistors in each of the two sources reduces the difference between the drain currents in the two transistor halves when the transconductance differs on the two transistor halves. We estimated the reduction in the difference between the drain currents of the two halves for the transistors under test. For typical values of $I_{DSS} \sim 70$ mA and $V_{TH} \sim$ −1.3 V at operating temperature, using separate 10 Ω ($2R_S$) resistor in each source, as in case (b), rather than connecting both sources to ground via a single 5 Ω (R_S) resistor, as in case (a), results in about 20% reduction in the sensitivity of the difference between the drain currents to device parameters. This separate biasing was implemented on Group 4 devices in Table 1.

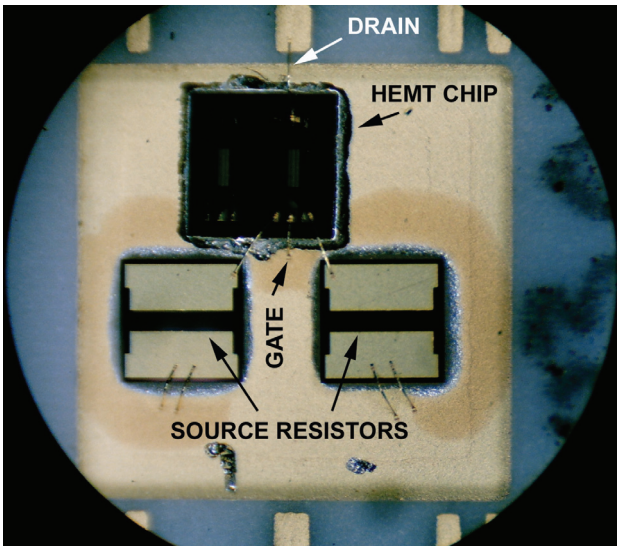

Figure 3 – Photograph of the wirebonding of a single two-source HEMT with two source resistors according to schematic shown in Figure 2.

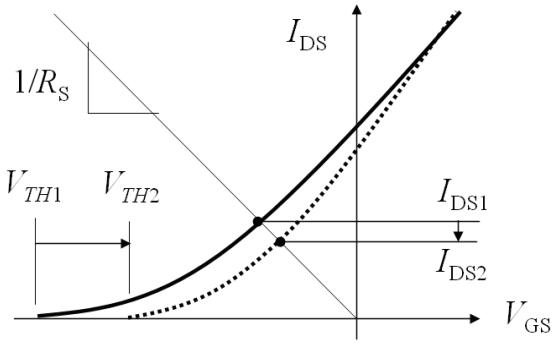

Figure 4 – The effect of transconductance or threshold voltage drift on measured drain current

The test system contained a number of 24V and 48V DC power supplies; one power supply and a dedicated analog panel ammeter per device. Analog meters offer practically infinite failure-free operation (no batteries) and no common electrical power supply lines. (Note that with the return path (ground) being common to all the devices in Figure 2, both

ammeter terminals have to be floating to make independent measurements of the drain current. The drain current data acquisition was done with no interruption to the device operation.

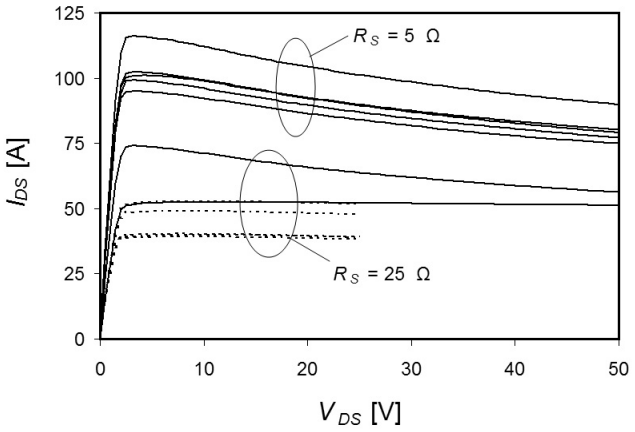

Figure 5 – Typical room-temperature DC characteristics (I_{DS} vs. V_{DS}) for devices under test connected using circuit diagram shown in Figure 12. The reduction in I_{DS} with voltage is due to self-heating and it is more pronounced for devices biased at 48V.

III. Results

The operating characteristics of the HEMTs can drift in many ways during a life test. Using the circuit layout shown in Figure 2, we are primarily sensitive to the changes in I_{DSS} and V_{TH}. We do not monitor gate leakage. Figure 4 illustrates how drift in V_{TH} and/or I_{DSS} affects the I_{DS} readout. Clearly, if I_{DSS} reduces with time, the readout I_{DS} will follow proportionally. If the threshold voltage V_{TH} changes, the transfer characteristics will shift and I_{DSS} will change again producing a change in the readout I_{DS}. In Figure 4, this is illustrated with I_{DS1} changing to I_{DS2} as V_{TH1} changes to V_{TH2}. The goal is to note any gross change in device characteristics and observe any catastrophic failures. Inasmuch as there was no prior knowledge of what the outcome of this test would be, the devices were planned for a range of different stress levels: The two different bias voltages V_{DS}, two different starting drain current levels I_{DS}, and two different package base temperatures T_B were grouped into four groups of conditions listed in Table 1.

The typical measured DC drain-to-ground characteristics are shown in Figure 5, where the gradual reduction with drain current is due to self-heating. The power dissipated on the source resistors (< 60 mW) is small in comparison with the power dissipated on the transistors as seen from Table 1. The thermal resistance on a sample device was measured using Liquid Crystal Thermography (LCT) [14] to be ≈17°C/W. The nematic-isotropic transition temperature of the liquid crystal used was T_{LC} = 136°C. Figure 6 shows the LCT measurement results: variation of power required to increase the temperature from the base temperature T_B to the T_{LC}. The slope of the linear regression line gives the thermal resistance $dP/dT_B = -\Theta_{TH}$. The data correlation coefficient was equal to 99.7%

Table 1 – Summary of conditions under which the devices were operated.

Group	Ch	T_B [°C]	I [mA]	R_S [Ω]	V_{DS} [V]	P [W]	T_{CH} [°C]
1	B7	152	32.5	25	24	0.73	164
	B8	152	31	25	24	0.70	164
	B9	152	34	25	24	0.76	165
	B10	152	30	25	24	0.68	163
2	A2	176	24.5	25	24	0.56	185
	A3	176	25	25	24	0.57	186
	A4	176	27.5	25	24	0.62	187
	A5	176	27.5	25	24	0.62	187
	A6	176	28	25	24	0.63	187
	A7	176	27.5	25	24	0.62	187
3	A15	176	34.5	25	48	1.60	203
	A16	176	30.5	25	48	1.42	200
	A18	176	33.5	25	48	1.55	202
4	A11	176	49	5	48	2.33	216
	A12	176	51	5	48	2.42	217
	A13	176	41.5	5	48	1.97	210
	A14	176	54	5	48	2.56	220
	A17	176	45	5	48	2.14	212
	A19	176	58	5	48	2.75	223
	A20	176	47.5	5	48	2.26	214

Due to different bias voltage and currents flowing though the devices, the power dissipated on the devices varied. Table 1 shows a list of devices currently on test with the bias conditions (V_{DS}, R_S, measured I_{DS} and power P), package base temperature (T_B) and estimated channel temperature ($T_{CH} = T_B + \Theta_{TH} \cdot P$). The power value in Table 1 has been corrected for the power dissipated on the source resistor R_S. Ten of the devices were operated at channel temperatures above 200°C with cumulative number of device hours above 175,000. The total number of device·hours for all devices is over 350,000. The data readout was performed manually which caused a certain amount fluctuation in the values read. The results for all devices tested are shown in Figure 7 where we start the plot after the burin-in time of 10 hours (time zero).

The results show that (a) no early failures nor catastrophic failures occurred in the first 17,500 hours of operation, and (b) the drift in the I_{DS} value was less than 10% of the starting value at time zero. If one interprets the no failure data to represent random failure portion of a failure-rate curve, i.e., cumulative failure distribution being exponential, one can estimate the upper bound on the failure rate. The upper bound on the (constant) failure rate with no failures is given by $\lambda = -\ln(1-CL)/nT$, where CL is the confidence level, n number of device under test, and T the time the devices were under test [15]. If we restrict our estimate only to the ten devices with

$T_{CH} \geq 200°C$, we find $\lambda \leq$ 2.7%/K for CL = 99% (K ≡ 1000 hrs). In other words, we are 99% confident that the failure rate on these devices would be less than 2.7% for every 1000 hours. Note that this is an *upper bound* on the failure rate for given confidence level and can be used only as an estimate of the lower bound on the mean time to failure (MTTF). Without any failures and a very limited range of channel temperatures used in the test, we do not attempt to estimate the activation energy. However, an estimate of the MTTF upper bound under normal operating conditions may be obtained if we assume activation energy E_A = 1.7 eV published on devices that have the same epilayer design as our devices [16]. If the devices under test were to exhibit the same failure mechanism as the as-grown AlGaN/GaN/Si transistors, at T_{CH} = 150°C the acceleration factor would be 137. This would result in an upper bound on the failure rate of 192 FIT. The MTTF for 200°C operation is >4.3 years with confidence 99%. If activation energy 1.7 eV is assumed, then the MTTF at 150°C reaches 600 years (>5·10^6 hours) for same confidence level.

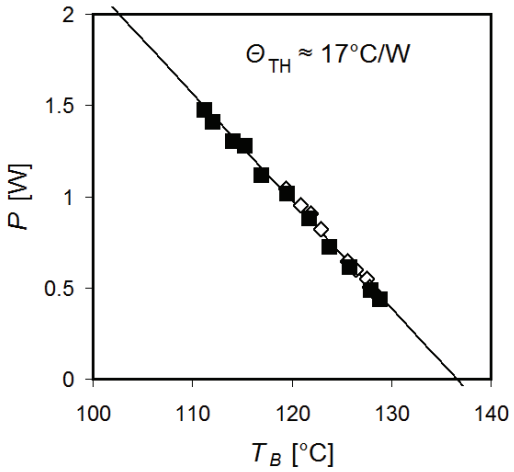

Figure 5 - Liquid crystal thermometry results at T_{LC} = 136°C.

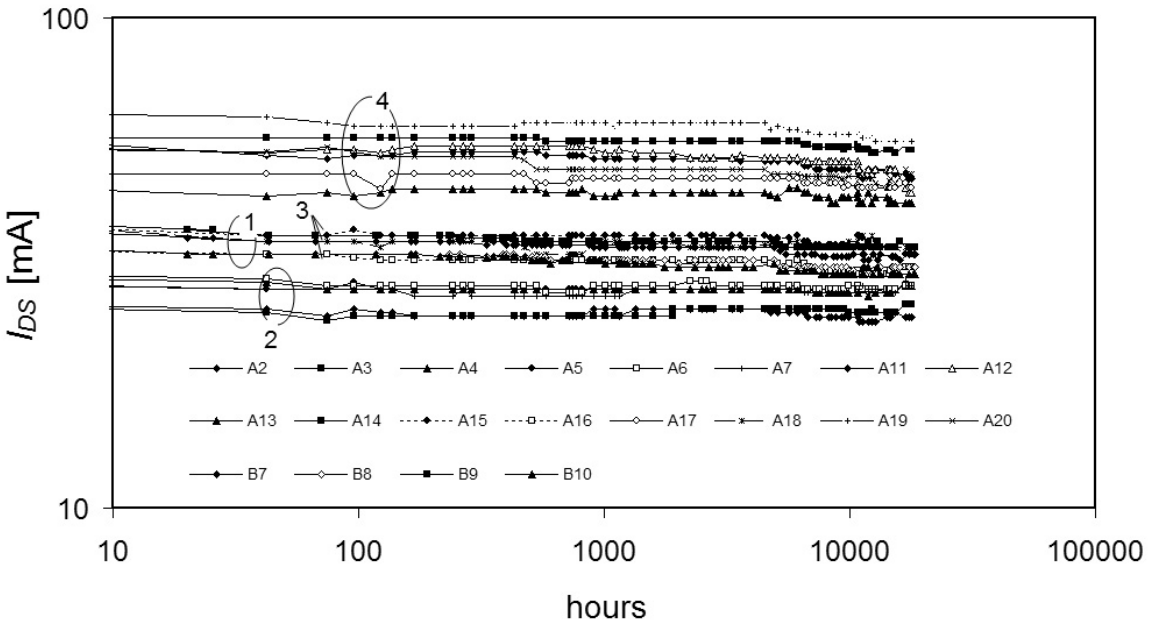

Figure 7 – I_{DS} versus time

I. Conclusions

GaN/Diamond technology using atomic attachment is progressing towards manufacturability. We have demonstrated that that transistors fabricated on these engineered wafers exhibit promising robustness: during 17,500 hours of operation the drift in drain current was less than 10% of the starting value in an experiment with 175,000 cumulative device-hours and estimated lower bound on MTTF of >5·10^6 hours.

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